REMARKS

General Objection

Claims 1 and 9

Claims 1 and 9 stand objected to under a general objection. In paragraph 1 on page 2 of the Office Action, the Examiner stated:

> Claim 9 states: "thereby limiting the leakage current of each of said transistors to a sub-threshold level even as said source voltage increases". According to this statement, an increase in the transistor current for bypassing an ESD transient cannot occur. The same conclusion can be drawn from a statement in Claim 1: "where the leakage current of said transistor is reduced to a sub-threshold level while an increasing source voltage applied at said source terminal reduces the gate-to-source voltage and reduces its threshold voltage". However, Claim 18 includes a limitation that overcomes this deficiency stating: "wherein a leakage current of said input protection transistors is controlled to a sub-threshold level over a range of voltages applied to each source terminal of said input protection transistors" (emphasis added). In other words, the transistor current is kept at subthreshold level only for voltages applied to the source terminals. Implicitly for voltages beyond the source terminals values the transistor current may increase, thus fulfilling its protection function. The same or similar limitations should be added to Claims 1 and 9. For purpose of examination it was assumed that the Claims 1 and 9 have the same limitations as the one in Claim 18.

In response to the Examiner's objection, Claims 1 and 9 have been rewritten to clearly state that under normal (non-ESD) bias condition the leakage current of the input protection is greatly reduced due to reverse source bias. Claim 1 now provides:

> 1. (currently amended) A device for electrostatic discharge input protection comprising:
>
> a transistor with gate, source, drain and substrate terminals;
>
> an input signal terminal coupled to said source terminal of said transistor;
>
> a reference point coupled to said gate and substrate terminals of said transistor;
>
> and

an ~~a~~ output signal terminal coupled to said drain terminal of said transistor;

where under a non-ESD bias condition the leakage current of the input protection is greatly reduced due to reverse source bias and the leakage current of said transistor is reduced to a sub-threshold level while an increasing source voltage applied at said source terminal reduces the gate-to-source voltage and reduces its threshold voltage.

Claim 9 now provides:

9. (currently amended) A low leakage Electrostatic Discharge (ESD) protection scheme comprising:

a plurality of low operating voltage devices, each device having at least one device input for receiving an input signal;

a plurality of input terminals for coupling an input signal to a device via a corresponding device input;

a plurality of transistors with gate, substrate, source and drain terminals,

each transistor providing an alternate pathway via a source terminal for signals from said plurality of input terminals; and

a reference coupled to corresponding gate and substrate terminals of said plurality of input protection transistors; and

a source voltage driving both said source terminals of said input protection transistors and said inputs of said low operating voltage devices;

wherein under a non-ESD bias condition the leakage current of the input protection is greatly reduced due to reverse source bias and ESD protection is achieved by coupling the source terminals of said plurality of transistors to said plurality of input terminals thereby limiting the leakage current of each of said transistors to a sub-threshold level even as said source voltage increases.

Claims 4, 13 and 24

Claims 4, 13 and 24 also stand objected to under a general objection. In paragraph 1 on page 2 of the Office Action, the Examiner objected to Claims 4, 13 and 24 due to the use of symbol "Vss". The Examiner stated:

> Even though it is common in EE sources to indicate the lowest potential supply terminal as Vss, its presence in the claim results in some uncertainty. A more definitive limitation should be used. For purpose of examination it was assumed that Vss stands for the lowest potential supply terminal.

In response to the Examiner's objection, the first full paragraph on page 8 of the Specification and Claims 4, 13, and 24 have been amended to reflect that Vss means the lower potential supply terminal.

Rejections Under 35 U.S.C. 112

Claims 6 and 15

Claims 6 and 15 stand rejected under 35 U.S.C. 112. On page 3 of the Office Action, the Examiner quotes the second paragraph of 35 U.S.C. 112.: The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention. In paragraph 2 on page 3 of the Office Action, the Examiner rejected Claims 6 and 15 under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as his invention. According to the Examiner, the following statements make the claims indefinite: "the resulting leakage current from said source voltage is approximately 10^{-14} $A/\mu m$". The Examiner states:

> The current is defined as amount of charge per cross sectional area (per squared value of length). Citation of current value in amperes per units of length makes the claims indefinite. Accordingly metes and bounds of the claim cannot be determined. The claim has not been treated with regard to prior art.

Applicant respectfully traverses Examiner's reasoning and rejection. Claims 6 and 15 are structured to address different protection levels (as determined by different device width) by normalizing the leakage on a per unit width basis. As such, the reference to 10^{-14} $A/\mu m$ in the

Claims 6 and 15 are definite and would be understood by those skilled in the art. Alternatively, the typical leakage value could have been referenced in Amperes/micron (um) of transistor width. Hence for a transistor with 100um of width, the typical leakage is less than 1pA (10^{e-14} * 100). In either case, the description particularly points out and distinctly claims the subject matter which Applicant regards as his invention.

Rejections Under 35 U.S.C. 102(b)

Claims 1, 5 and 8

Claims 1, 5 and 8 stand rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 5,903,419 to Smith ("Smith"). On page 3 of the Office Action, Examiner quotes 35 U.S.C. 102(b): A person shall be entitled to a patent unless (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States. In paragraph 3 on page 3 of the Office Action, Examiner states:

> Smith discloses an ESD protection having a transistor with gate, source, drain and substrate terminals (element 204 in Fig. 2), an input terminal coupled to the source terminal of the transistor (I/0 PAD 14 in Fig. 2), a reference point coupled to the gate and substrate terminals of the transistor (Vdd in Fig. 2), and an output signal terminal coupled to the drain terminal of the transistor (base of transistor 202 is coupled to the drain of transistor 204 in Fig. 2). Due to a diode (element 206 in Fig. 2), a gate to substrate voltage is always positive, which moves the PMOS transistor into sub-threshold regime. Increase of the transistor source voltage reduces the source-to-gate threshold. One of the goals of the invention in the reference is a reduction of a leak current (col. 2, lines 20 - 29, col. 4, lines 1 -5, col. 9, lines 25 -35). Regarding Claim 5, Smith discloses the device having the source voltage of a few hundreds millivolts (a voltage drop across diode 206 in Fig. 2). Regarding Claim 8, discloses a PMOS transistor (element 204 in Fig. 2).

As for Claims 1, 5 and 8, Applicant respectfully traverses the Examiner's rejection and reasoning. Smith discloses an electrostatic discharge (ESD) circuit wherein a discharge path is provided by a parasitic bipolar transistor (202). The parasitic bipolar device is triggered by a combination of a MOSFET (204) and a string of diodes (200). The trigger point of the MOSFET is

programmable by varying the number of individual diodes in the string of diodes. A feedback circuit (602) ensures that MOSFET (204) is in a conductive state independent of the voltage state of the voltage supply, VDD, during an ESD event. (see Abstract). As is evident in foregoing description and in the claims of Smith, Smith proposes a concept of ESD protection that does not achieve low current leakage. It is instructive to note that the architecture of Smith is substantially and significantly different than that of the present invention as claimed in Claim 1, 5 and 8. For a prior-art reference to anticipate under 35 U.S.C. Section 102, every element of the claimed invention must be identically shown in a single reference. These elements must be arranged as in the claimed under review. *In re Bond*, 15 U.S.P.Q.2d 1566, 1567-68 (Fed. Cir. 1990). As such, Smith cannot anticipate Claim 1 or any of its respective dependent claims, including Claims 5 and 8.

Simulations show that when applied under the same manufacturing technology, the invention of Smith experiences current leakage at least 100 times more than that of the present invention. As such, these two inventions have very different levels of performance.

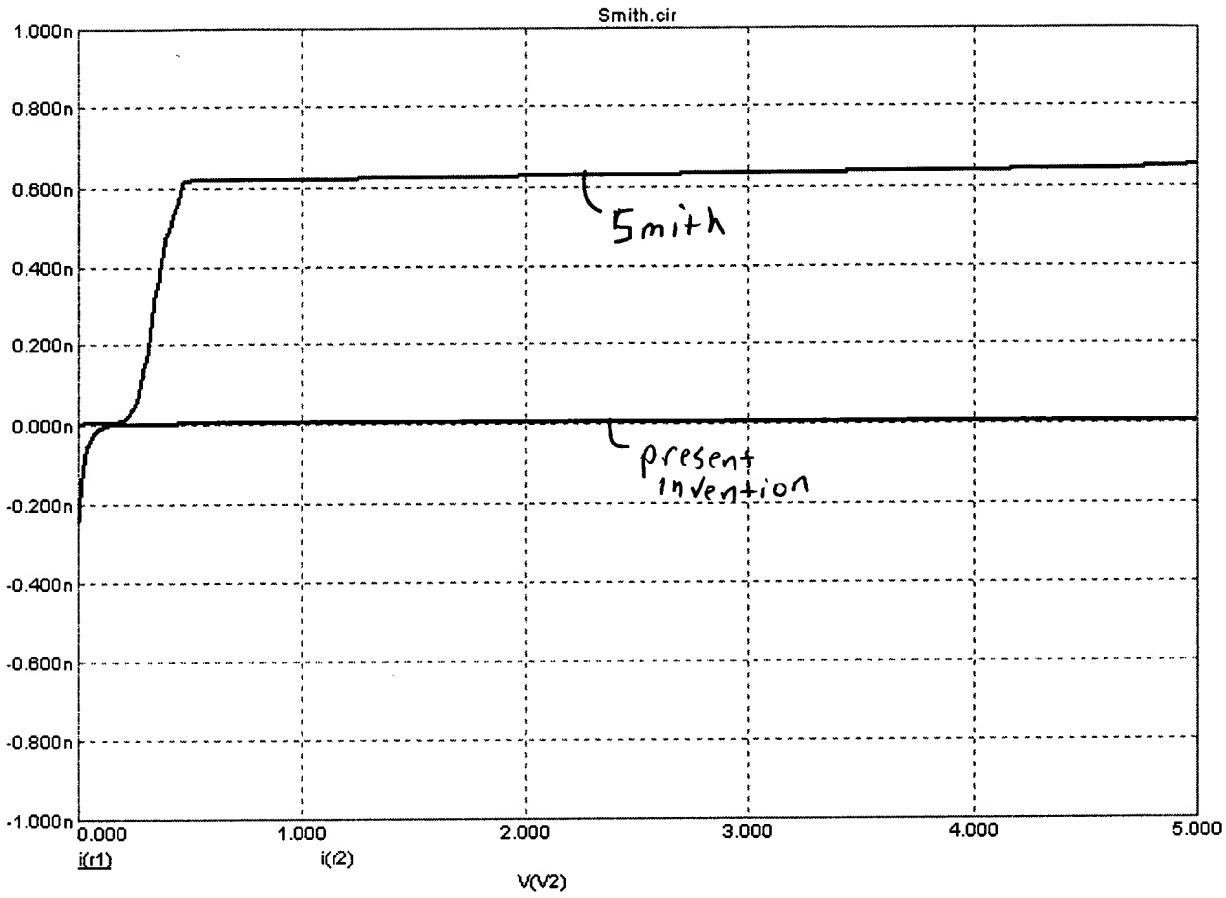
Examiner states that Smith discloses reverse biasing the source to reduce leakage in the I/O protection. Applicant respectfully responds that detailed analysis of the invention of Smith shows that this reverse bias is only possible if current is already flowing through the PMOS transistor 204 (of Smith) and through the diodes 200 (of Smith). Furthermore this current flows through the base of the bipolar transistor 202 (of Smith). The leakage in the invention disclosed in Smith is much higher because the leakage through the PMOS transistor 204 (of Smith) is feeding the base of the bipolar transistor 202 (of Smith) thus generating a collector current about 100 time greater, which is drawn from the I/O pad 14 (of Smith).

The proper functioning of the invention of Smith requires a very good bipolar transistor with very low Ron (~1Ohm) and fast transit times (<10nSec). Such NPN transistors are not available on regular CMOS technology but rather on BiCMOS technology. The description of Smith either does not account for all the physics occurring during the ESD event and the invention does not function as described or the description fails to clearly describe all conditions under which the invention is functioning and which would severely weaken it. In addition, Smith discloses (Col.8 line 14) that diode 206 (of Smith) can be replaced with a short, whereas Examiner states that diode 206 (of

Smith) is used to create part of the reverse bias. In light of Smith's admission that diode 206 (of Smith) can be replaced with a short, diode 206 (of Smith) has little, if any use, in the embodiment of Fig. 2 as applied to Claims 1, 5 and 8 of the present invention.

The invention of Smith appears to use isolated diodes 200 (of Smith), however the description in Smith does not disclose how these diodes are constructed. In effect, it is impossible using CMOS technology to create isolated diodes, although they can be fabricated using poly-silicon. Such diodes have high current leakage and very high series resistance, in the KOhm range typically, which renders them substantially inferior for ESD protection. For example, a 2KeV ESD stress applies a 2.6Amps stress through an input protection device. In order to maintain on-chip voltages below 10-20V, a series resistance of less than 10 Ohms is necessary. The disclosure of Smith does not describe how such low resistance is achieved. As disclosed in the present invention low resistance is obtained because, during the ESD event, the MOS transistor goes into snap-back and possibly secondary snap-back. General ESD protection concepts are not discussed in the present invention as these are well known in the art.

To further illustrate that the invention of Smith is substantially, and significantly different from the present invention, in the Smith invention current must to flow through the PMOS transistor and diodes to provide the reverse bias. Also, the invention of Smith is much more complex inasmuch as the Smith invention requires at least eight (8) components and is sensitive to the manufacturing technology. In contrast, the present invention only requires one (1) components and is not manufacturing technology dependent. In operation, the present invention differs substantially from the present invention. The present invention requires no DC current to bias the I/O protection transistor such that the source junction is reversed biased. As a result, the invention of Smith has leakage much higher than the present invention and thus the Smith invention is not usable in ultra-low-leakage applications. Below is a graph of the simulated I/O protection for the Smith invention and the protection of the present invention. As can be seen, the present invention as claimed in Claims 1, 5 and 8 perform much better from a leakage view point.



Rejections Under 35 U.S.C. 103(a)

Claims 7, 2, 3 and 4

Claims 7, 2, 3, and 4 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Smith in view of the A. Sedra and K. Smith textbook "Microelectronic Circuits" ("Sedra Textbook"). Examiner quotes 35 U.S.C. 103(a):

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

In paragraph 4 on page 4 of the Office Action, Examiner states:

> Smith discloses all the elements of Claim 1. However, regarding Claim 7, it does not disclose the NMOS transistor. According to the Microelectronic Circuits textbook (pages 3442 -343), the NMOS and PMOS transistors are equivalents and are interchangeable. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have used NMOS transistor as equivalent replacement for PMOS transistor, because as the textbook states (pages 243 -343), they are equivalents and interchangeable. Selection of particular type of transistor is a designer decision, which is far from being an inventive step.

As for Claims 7, Applicant respectfully traverses the Examiner's rejection and reasoning. As noted above, Smith does not disclose all the elements of Claim 1. Smith discloses an electrostatic discharge (ESD) circuit wherein a discharge path is provided by a parasitic bipolar transistor (202). The parasitic bipolar device is triggered by a combination of a MOSFET (204) and a string of diodes (200). The trigger point of the MOSFET is programmable by varying the number of individual diodes in the string of diodes. A feedback circuit (602) ensures that MOSFET (204) is in a conductive state independent of the voltage state of the voltage supply, VDD, during an ESD event. (see Abstract). As is evident in foregoing description and in the claims of Smith, Smith proposes a concept of ESD protection that does not achieve low current leakage. It is instructive to note that the architecture of Smith is substantially and significantly different than that of the present invention as claimed in Claim 1, from which Claim 7 depends.

Further, regarding Claims 2, 3 and 4, the Examiner states:

> Smith discloses the reference point (element Vdd in Fig. 2), which for PMOS transistor plays the same role as the ground, or Vss (the lowest potential) voltage for NMOS transistor. Therefore, for the equivalent PMOS transistor the reference potential is equal Vdd volts, rather than 0 volts.

As for Claims 2, 3 and 4, Applicant respectfully traverses the Examiner's rejection and reasoning. As noted above, Smith does not disclose all the elements of Claim 1. The architecture of Smith is substantially and significantly different than that of the present invention as claimed in Claim 1, from which Claims 2, 3 and 4 depend.

Combination of References

The **combination** of Smith and the Sedra Textbook fails to render the claimed invention in Claims 7, 2, 3 and 4 obvious. The architecture and objectives of the Smith invention are significantly and substantially different from that claimed in Claims 7, 2, 3 and 4. Furthermore, neither invention of Smith, nor the general interchangeability of PMOS transistors and NMOS transistors as described in the Sedra Textbook gives rise to any suggestion or incentive in either reference to combine the references so as to arrange the elements in the manner described in Claim 1, from which claims 7, 2, 3 and 4 depend. Thus, without using hindsight of selective picking and choosing, Applicant respectfully submits that the combination of the references falls short of rendering obvious the claimed invention.

In discussing a rejection under 35 U.S.C. 103, the Court, in *In re Wesslau*, 147 U.S.P.Q. 391, 393 (C.C.P.A. 1965) held that:

> It is impermissible within the framework of Section 103 to pick and choose from any one reference only so much of its as will support a given position, to the exclusion of other parts necessary to the full appreciation of what such reference fairly suggests to one of ordinary skill in the art.

The Examiner may not use Applicant's claims as a blueprint to pick and choose from one of the references only so much of it as will support the Examiner's position and to exclude other parts necessary to the full appreciation of what that reference fairly suggests to one of ordinary skill in the art. This type of piecemeal reconstruction of the references in light of Applicant's disclosure is not a permissible basis for holding the invention obvious. *In re Kamm and Young*, 172 U.S.P.Q. 298, 301-302 (C.C.P.A. 1972).

The Federal Circuit has repeatedly held that hindsight must be avoided in combining reference structures. *Panduit Corp. v. Dennison Manufacturing Co.*, 227 U.S.P.Q. 337, 343 (Fed. Cir. 1985); *In re Find*, 5 U.S.P.Q.2d 1596, 1599-1560 (Fed. Cir. 1988). Thus, it is error to reconstruct a patentee's claimed invention from the prior art by using the patentee's claims as a blueprint. Prior art references must be read as a whole and consideration must be given where the references diverge and teach away from the claimed invention. *W.L. Gore & Associates, Inc. v.*

Garlock, Inc., 220 U.S.PQ. 303, 311-13 (Fed. Cir. 1983). A claim cannot properly be used as a blueprint for abstracting individual teachings from references. *Ashland Oil, Inc. v. Delta Resins & Refractories, Inc.*, 227 U.S.P.Q. 657, 667 (Fed. Cir. 1985).

Claims 9, 14, 17, 18 and 20

Claims 9, 14, 17, 18 and 20 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Watt et al. (U.S. Pat.No. 5,751,507) ("Watt") in view of Smith. Regarding Claims 9 and 18, Examiner states:

> ...Watt et al. discloses an ESD protection solution for a plurality of low operating voltage devices having a plurality of input terminals (input pads 1, 2, ... N in Fig. 2). Each input has its own ESD protection (elements D1 and D3 in Fig. 2).
>
> However, he does not disclose a low leakage current solution for ESD protection devices. Smith discloses an ESD protection having a transistor with gate, source, drain and substrate terminals (element 204 in Fig. 2), an input terminal coupled to the source terminal of the transistor (I/0 PAD 14 in Fig. 2), a reference point coupled to the gate and substrate terminals of the transistor (Vdd in Fig. 2), and an output signal terminal coupled to the drain terminal of the transistor (base of transistor 202 is coupled to the drain of transistor 204 in Fig. 2). Due to a diode (element 206 in Fig. 2), a gate to substrate voltage is always positive, which moves the PMOS transistor into subthreshold regime. Increase of the transistor source voltage reduces the source-to-gate threshold. One of the goals of the invention in the reference is a reduction of a leak current (col. 2, lines 20 - 29, col. 4, lines 1 -5, col. 9, lines 25 -35). Both patents have the same problem solving area, namely providing an efficient ESD protection for integrated circuits. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have used the plurality of transistors according to Smith protecting each of the inputs of the Watt et al. circuit, because as well known in the art and stressed by Smith (col. 2, lines 20 - 29), the leakage current presents a problem in many electronic circuits, especially in a view that they increase with a temperature.

As for Claims 9 and 18, Applicant respectfully traverses the Examiner's rejection and reasoning. Claim 9, as amended, is set forth above. Claim 18 of the present invention provides:

> 18. (original) A low voltage Integrated Circuit (IC) with on-board ESD input protection comprising:

a plurality of low operating voltage devices,

at least one reference point, one supply voltage point and a plurality of input terminals coupled to said devices;

a plurality of input paths for coupling input signals to said devices via said input terminals; and

a plurality of input protection transistors with gate, substrate, source, and drain terminals arranged between said input paths and said devices, each source terminal coupled to a corresponding input path, each gate and substrate terminal coupled to a reference point;

wherein a leakage current of said input protection transistors is controlled to a sub-threshold level over a range of voltages applied to each source terminal of said input protection transistors.

The description and operation of the Smith invention is described above. The analysis and differentiation of the Smith invention under the discussion of Claims 1, 5, and 8 of the present invention are incorporated herein by reference. Watt discloses an apparatus for protecting an integrated circuit against damage from electrostatic discharges (ESD), which includes a single ESD bus that is connected to multiple input pads through a respective diode. The ESD bus is isolated from the positive power supply bus V_{DD}. The ESD bus is coupled to the negative power supply bus Vss by a FET-triggered SCR circuit. ESD charge on an input pad forward biases the respective diode and charges the ESD bus. When the voltage of the ESD bus reaches a predetermined threshold voltage, the FET breaks down, and triggers the SCR circuit to shunt the charge on the ESD bus to V_{SS}. The threshold voltage is selected such that, in normal operation, voltages higher than V_{DD} may be applied to the input pad without input leakage current.

The **combination** of Smith and Watt fails to render the claimed invention in Claims 9 and 18 obvious. Smith does not disclose all the elements of Claim 9 or Claim 18. The architecture and objectives of Smith are substantially and significantly different than that of the present invention as claimed in Claims 9 and 18. Furthermore, neither invention of Smith, nor the invention of Watt give

rise to any suggestion or incentive in either reference to combine the references so as to arrange the elements in the manner described in Claims 9 or 18. The case law interpreting the proper use of references for 35 U.S.C. 103(a) purposes as set forth under the discussion of Claims 7, 2, 3 and 4 of the present invention is incorporated herein by reference. Thus, without using hindsight of selective picking and choosing, Applicant respectfully submits that the combination of the references falls short of rendering obvious the claimed invention.

Regarding Claim 14, Examiner states:

Smith discloses the device having the source voltage of a few hundreds millivolts (a voltage drop across diode 206 in Fig. 2).

Claim 14 of the present invention provides:

14. (original) The protection scheme of claim 9 wherein said source voltage is limited to a few 100mV.

As for Claim 14, Applicant respectfully traverses the Examiner's rejection and reasoning. The **combination** of Smith and Watt fails to render the claimed invention in Claim 14 obvious. The architecture and objectives of the Smith invention are significantly and substantially different from that claimed in Claim 14. The analysis and differentiation of the Smith invention under the discussion of Claims 1, 5, and 8 of the present invention are incorporated herein by reference. Furthermore, neither invention of Smith, nor the invention of Watt gives rise to any suggestion or incentive in either reference to combine the references so as to arrange the elements in the manner described in Claim 14. The case law interpreting the proper use of references for 35 U.S.C. 103(a) purposes as set forth under the discussion of Claims 7, 2, 3 and 4 of the present invention is incorporated herein by reference. Thus, without using hindsight of selective picking and choosing, Applicant respectfully submits that the combination of the references falls short of rendering obvious the claimed invention.

Regarding Claims 17 and 20, Examiner states: [Smith] "discloses a PMOS transistor (element 204 in Fig. 2)."

Claim 17 provides:

17. (original) The protection scheme of claim 9 wherein said plurality of transistors are PMOS type.

Claim 20 provides:

20. (original) The IC of claim 18 wherein said plurality of input protection transistors are PMOS type.

As for Claims 17 and 20, Applicant respectfully traverses the Examiner's rejection and reasoning. The **combination** of Smith and Watt fails to render the claimed invention in Claims 17 (which depends on Claim 9) or 20 (which depends on Claim 18) obvious. The architecture and objectives of the Smith invention are significantly and substantially different from that claimed in Claims 17 and 20. The analysis and differentiation of the Smith invention under the discussion of Claims 1, 5, and 8 of the present invention are incorporated herein by reference. Furthermore, neither invention of Smith, nor the invention of Watt gives rise to any suggestion or incentive in either reference to combine the references so as to arrange the elements in the manner described in Claims 17 or 20. The case law interpreting the proper use of references for 35 U.S.C. 103(a) purposes as set forth under the discussion of Claims 7, 2, 3 and 4 of the present invention is incorporated herein by reference. Thus, without using hindsight of selective picking and choosing, Applicant respectfully submits that the combination of the references falls short of rendering obvious the claimed invention.

Claim 10

Claim 10 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Watt et al. in view of Smith and further in a view of Ker et al. article "Capacitor-Coupled ESD Protection Circuit for Deep-Submicron Low-Voltage CMOS ASIC" (the "Ker Article"). In paragraph 6 on page 6 of the Office Action, the Examiner states:

> As was stated above, Watt et al. and Smith disclose all the elements of Claim 9. However, regarding Claim 10, they do not disclose the solution according to teachings of Watt et al. and Smith being used for protection of the low voltage CMOS circuit. Ker et al. discloses an ESD protection for the low voltage CMOS circuit. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have used the solution according to teachings of Watt et al. and Smith for protection of the low voltage CMOS circuit, because as Ker et al. state (see Operating Principles pages 310- 311), the submicron low voltage CMOS circuits more than other circuits need the ESD protection.

As for Claim 10, Applicant respectfully traverses the Examiner's rejection and reasoning. As noted above, Watt and Smith fail to disclose all the elements of Claim 9, from which Claim 10 depends. The analysis and differentiation of the Smith invention under the discussion of Claims 1, 5, and 8 of the present invention are incorporated herein by reference. Further, the Ker Article proposes a capacitor-coupled technique used to lower snapback-trigger voltage and ensure uniform ESD current distribution in deep-submicron CMOS on-chip ESD protection circuit. The coupling capacitor is realized by a poly layer under the wire-bonding metal pad without increasing extra layout area to the pad. A timing-original design model has been derived to calculate the capacitor-couple efficiency of the Ker proposed ESD protection circuit. According to Ker, using this capacitor-coupled ESD protection circuit, the thinner gate oxide of CMOS devices in deep-submicron low-voltage CMOS ASIC can be effectively protected. None of the invention of Smith, Watt or the Ker Article gives rise to any suggestion or incentive in any of such reference to combine the references so as to arrange the elements in the manner described in Claims 9 or 10. The case law interpreting the proper use of references for 35 U.S.C. 103(a) purposes as set forth under the discussion of Claims 7, 2, 3 and 4 of the present invention is incorporated herein by reference. Thus, without using hindsight of selective picking and choosing, Applicant respectfully submits that the combination of the references falls short of rendering obvious the claimed invention.

Claims 16, 19, 11-13 and 22-24

Claims 16, 19, 11-13 and 22-24 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Watt in a view of Smith and further in view of the Sedra Textbook. In paragraph 7 on page 7 of the Office Action, the Examiner states:

> As was stated above, Watt et al. and Smith disclose all the elements of Claim 9. However, regarding Claims 16 and 19, they do not disclose the NMOS transistor. According to the Microelectronic Circuits textbook (pages 3442 -343), the NMOS and PMOS transistors are equivalents and are interchangeable. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have used NMOS transistor as equivalent replacement for PMOS transistor, because as the textbook states (pages 243 -343), they are equivalents and interchangeable. Selection of particular type of transistor is a designer decision, which is far from being an inventive step.

As for Claims 16, 19, 11-13 and 22-24, Applicant respectfully traverses the Examiner's rejection and reasoning. Watt and Smith fail to disclose all the elements of Claim 9, from which Claims 16, and 11-13 depends. The analysis and differentiation of the Smith invention under the discussion of Claims 1, 5, and 8 of the present invention are incorporated herein by reference. Further, as noted above, the inventions of Smith and Watt are significantly and substantially different from the present invention, both in their architectures and in operation Therefore, the further element regarding the interchangeability of NMOS and PMOS, coupled to the foregoing references does not support a given position, to the exclusion of other parts necessary to the full appreciation of what such reference fairly suggests to one of ordinary skill in the art. The case law interpreting the proper use of references for 35 U.S.C. 103(a) purposes as set forth under the discussion of Claims 7, 2, 3 and 4 of the present invention is incorporated herein by reference. Without using hindsight of selective picking and choosing, Applicant respectfully submits that the combination of the references falls short of rendering obvious the claimed invention.

Claims 11-13 and 22-24

Claims 11-13 and 22-24 further stand rejected under 35 U.S.C. 103(a) as being unpatentable over Watt in a view of Smith and further in view of the Sedra Textbook. In paragraph 7 on page 7 of the Office Action, the Examiner further states:

> Regarding Claims 11-13 and 22-24, Smith discloses the reference point (element Vdd in Fig. 2), which for PMOS transistor plays the same role as the ground, or Vss voltage for NMOS transistor. Therefore the reference potential is equal Vdd volts, rather than 0 volts.

As for Claims 11-13 and 22-24, Applicant respectfully traverses the Examiner's rejection and reasoning. The analysis and differentiation of the Smith invention under the discussion of Claims 1, 5, and 8 of the present invention are incorporated herein by reference. Watt and Smith fail to disclose all the elements of Claim 9, from which Claims 11-13 depend, and Claim 18 from which Claims 11-13 depend. Further, as noted above, the inventions of Smith and Watt are significantly and substantially different from the present invention, both in their architectures and in operation Therefore, the fact that Smith discloses that the reference potential is equal to Vdd volts, rather than 0 volts, coupled to the foregoing references does not support a given position, to the exclusion of other parts necessary to the full appreciation of what such reference fairly suggests to one of ordinary skill in the art. The case law interpreting the proper use of references for 35 U.S.C. 103(a) purposes as set forth under the discussion of Claims 7, 2, 3 and 4 of the present invention is incorporated herein by reference. Without using hindsight of selective picking and choosing, Applicant respectfully submits that the combination of the references falls short of rendering obvious the claimed invention.

Other References Not Relied Upon

The prior art made of record by the Examiner and not relied upon which is considered pertinent to applicant's disclosure are U.S. Pat. No. 6,144,542 ("Ker I"), U.S. Pat. No. 6,249,410 ("Ker II"), U.S. Pat. No.5,852,541 ("Lin I") and U.S. Pat. No. 5,959,488 ("Lin II"). Applicant respectfully responds that none of the foregoing references, alone or in combination, anticipate the present invention or make the invention unpatentable under 35 U.S.C. 103(a).

As noted herein and in the application of the present invention, the present invention is directed toward a novel architecture of a ESD protection circuit that achieves low leakage currents.

Ker I discloses a whole-chip ESD protection scheme with the ESD buses designed to solve the ESD protection issue of the CMOS IC having a large number of separated power lines. Multiple ESD buses, which are formed by the wide metal lines, are added into the CMOS IC having a large number of separated power lines. The bi-directional EDS-connection cell are connected between the separated power lines and the ESD buses, but not between the separated power lines. The ESD current on the CMOS IC with more separated power lines are all conducted into the ESD buses, therefore the ESD current can be conducted by the ESD buses away from the internal circuits and quickly discharged through the designed ESD protection devices to ground.

Ker II discloses an ESD protection circuit connected to an integrated circuit operable to dissipate an electrostatic charge from an ESD source placed in contact with two terminals of the integrated circuit to prevent damage to the integrated circuits. The ESD protection circuit has a ESD shunting circuit for shunting the electrostatic charge from integrated circuit. The ESD shunting circuit has a first port connected to one terminal of the integrated circuit, a second port connected to another terminal of the integrated circuit, and a third port. The ESD protection circuit additionally has an ESD detection circuit. The ESD detection circuit has a first input port connected to the one terminal of the integrated circuit, a second input port connected to the other terminal of the integrated circuit, and an output port connected to the third port of the ESD shunting circuit. When the ESD detection circuit detects the presence of the electrostatic charge from the ESD source, the ESD detection circuit generates an excess voltage at the third port that will damage the ESD shunting circuit. Finally the ESD protection circuit has a voltage clamping circuit connected between the third port of the ESD shunting circuit and one of the terminals of the integrated circuit to prevent the generation of the excess voltage at the third port of the ESD shunting circuit.

Lin I discloses a transient oscillating circuit operable to generate a series of current pulses for triggering turn-on of an ESD protection device. As VDD-to-VSS voltage increases rapidly in the initial ESD event, the series of current pulses injects minority carriers into the p-well of an NMOS transistor via an adjacent n+/p-well diode. The minority carriers flow toward the drain-substrate

junction of the NMOS transistor such that the NMOS transistor is triggered at a trigger voltage lower than that provided by the prior art. According to Lin I, the invention improves the ESD performance of an ESD protection device, such as a MOSFET or bipolar transistor, which is provided for protecting the power bus or IC pins during an ESD event.

Lin II discloses a dual-node capacitor coupling technique used to lower the trigger voltage and to improve the uniform turn-on of a multi-finger MOSFET transistor. In Lin II, preferably, each MOSFET is an NMOS device. Specifically, each NMOS device includes a capacitor that is connected between the gate of the NMOS device and the pad terminal. A first resistor is connected between the gate and the p-well, while a second resistor is connected between the p-well and the grounded source. For a positive ESD pulse to VSS, the p-well is pulled up to approximately 0.7 V during the initial ESD event, such that the source junction is forward biased and that the trigger voltage of the NMOS device is lowered. At the same time, the gate voltage is coupled within the range of approximately 1 to 2 V to promote the uniform turn on of the gate fingers of the NMOS devices during the initial ESD event.

Conclusion

Applicant respectfully submits that Claims 1-24, now pending, are in condition for allowance. A Notice of Allowance is therefore requested.

If the Examiner has any other matters which pertain to this Application, the Examiner is encouraged to contact the undersigned to resolve these matters by Examiner's Amendment where possible.

Favorable consideration of the pending claims is respectfully requested.

Respectfully Submitted,

Michael G. Cameron
Reg. No. 50, 298

Date: June 11, 2003

Jackson Walker L.L.P.
2435 North Central Expressway, Suite 600
Richardson, TX 75080
Tel: (972) 744-2902
Fax: (972) 744-2909

VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Specification:

Please replace the first full paragraph of page 8 of the Specification (lines 8 through 21) with the following:

With reference now to Figure 2A, therein is shown an ESD input protection device 80, according to the invention. The device 80 comprises a transistor 82, or other similar field effect device, with a source terminal 100 connected directly to input path 12 which, in turn, is connected to pad 16. The device to be protected (not shown) has an input terminal 14 which is likewise coupled to path 12. The drain terminal 102 of the transistor 82 is shown coupled to drain voltage (V_{dd})while the gate 103 and substrate 104 terminals are connected to reference. In particular, substrate terminal 104 is connected to reference point 106 which may be the supply voltage (V_{SS}), ground, or zero volt reference of the ESD application. Thus, the input signal from the source voltage 18 is directly connected to the source terminal 100 of transistor 82. Likewise, the gate terminal 103 is connected to reference 107 which may be the identical to reference 106 (supply voltage (V_{SS},), ground, or zero volt reference) or just the reference of the ESD application. For purposes of clarity, Vss refers to the lowest potential supply voltage.